REMARKS

Claims 2-14 and 16-19 will be pending upon entry of the present amendment. Claims 1 and 15 are being canceled. Claims 2, 8, 11, 16, and 19 are being amended.

The applicants appreciate the indication that claims 2-7, 11-14, and 16-19 are directed to allowable subject matter. Accordingly, claims 2, 11, 16, and 19 are being placed in independent form, and thus, are allowable. Claims 3-7, 12-14, and 17-18 depend on claims 2, 11, and 16, respectively, and thus, are also allowable.

Claims 1-19 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification in a way to enable one to make and use the invention. The drawings were objected to for similar reasons. In particular, the Examiner questions how Vref is generated and questions whether there should be a dot connection between Vref and the collector of transistor Q2

The applicant submits that the specification properly enables one skilled in the art to make and use the invention. Pages 2-3 explain in detail how the bandgap reference voltage Vref of Figure 1 is generated. One skilled in the art would recognize that the generation of Vref at the bases of Q1 and Q2 would occur similarly to that described on pages 2-3 with respect to Figure 1 because the transistors Q1 and Q2 are connected similarly in both figures.

In particular, Vref is generated as follows in Figure 5. The current mirror 6 forces the collector currents of Q1 and Q2 to be the same (= I1). Under this condition the voltage across R1 is the difference between the base-emitter voltages of Q1 and Q2: V(R1) + Vbe1 – Vbe2. From the transistor base equation:

$$I(\text{collector}) = n * Io * \exp(Vbe/Vt),$$

$$V(R1) = Vt * \ln(I1/Io) - Vt * \ln(I1/(M * Io)),$$

$$V(R1) = Vt * \ln(M), \text{ and}$$

$$V(R1 = (k/q) * T * \ln(M),$$

where:

M is the ratio of the area of Q2 to Q1,

k is boltzman's constant, and

q is the unit of electric charge.

The current through R1 is the same as I1 if we assume that the base current of Q1 and Q2 are very small. Then, Vref can be written as:

$$Vref = V(R2) + V(R1) + Vbe2,$$

$$Vref = V(R2) + Vbe1,$$

$$Vref = 2 * I1 + Vbe1,$$

$$Vref = 2 * (K/q) * T * \ln(M) + Vbe1.$$

The first term in the right side of the last equation is proportional to T (absolute temperature) whereas the second term has a negative temperature coefficient. These two terms are combined such that the Vref does change significantly over temperature.

The above equations show that no connection is necessary between Vref and the collector of either of the transistors Q1 and Q2. The voltage Vref is function of the base-emitter voltage Vbe1 of the transistor Q1 and does not necessarily equal the collector voltage of Q1.

For the foregoing reasons, claims 1-19 are properly supported by an enabling disclosure and no change needs to be made to Figures 1 and 5.

Claims 8-14 were rejected under 35 U.S.C. § 112, first paragraph, as not be supported by an enabling disclosure. In particular, the Examiner asserted that some structure corresponding to the current mirror 6, bandgap reference circuit 8, and comparator 4 of Figure 5 is deemed critical to the invention, but is not included in the claims.

Claim 8 is being amended to include a current source, reference voltage circuit, and comparator. It is not necessary for those structures to correspond identically to the structures of Figure 5, although the structures of Figure 5 provide a working example of the claimed invention. Claim 11 already included an output comparator, a reference voltage circuit, and a second current mirror, and thus, claim 11 is not being amended in that respect. Claims 9-10 and 12-14 depend on claims 8 and 11, respectively. Accordingly, amended claims 8-14 are supported by an enabling disclosure.

Claims 1-19 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In particular, the Examiner asserted that there is no support for the first circuit being "to measure Vref." Although the applicants submit that claim 1 did not recite that the first circuit measured Vref, and instead recited that the reference voltage line was connected to measure

Vref, claim 2 is being amended to recite that the reference voltage line is connected to supply Vref to the output comparator.

In addition, the Examiner asserted that there is no support for the language of lines 8-9 of claim 1 because the second current mirror does not supply two input currents. The applicant disagrees because the current mirror 7 of Figure 5 does provide two current inputs: a first current I2 is supplied to the sense resistor R3 and a second current I2 is supplied to the node connected the collector of transistor Qb to the collector of transistor Qc. Both of the currents I2 are in the same direction and both are properly called input currents to the sensing device and the compensation circuit. Further, even if the currents are in opposite directions, there is nothing wrong with calling them current inputs because current inputs can be positive or negative.

The Examiner also asserted that lines 10-14 of claim 1 do not recite where the "current gain" is provided. Again, the applicant disagrees. Claim 1 recited that the current gain provided is the ratio of the second current input to the first current input. That is, the compensation circuit causes a gain between the first and second current inputs.

For the foregoing reasons, claims 2-7 particularly point out and distinctly claim the invention.

With respect to claim 8, the Examiner asserts that there is no function or purpose recited for the "compensation circuit." The applicant submits that there is no requirement for the claim to recite a function or purpose. It is sufficient for the claim structures to have a function or purpose, which would be clear to one skilled in the art in view of the discussion in the specification.

The Examiner rejected claims 15-19 for similar reasons to those discussed above with respect to claim 1. As a result, claims 16-19 particularly point out and distinctly claim the invention for reasons similar to those discussed above.

Claims 8-10 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,961,215 to Lee et al. ("Lee").

Lee does not disclose the invention recited in claim 8. Claim 8 recites a thermal sensor circuit with a compensation circuit that includes first, second, and third transistors having respective control terminals coupled to each other. An example of such an arrangement can be

seen in the transistors Qa, Qb, Qd of Figure 5. Lee does not disclose three transistors with their control terminals coupled together. The Examiner points to transistors 40, 42, 50, and 52 as being a compensation circuit, but the gates of transistors 40 and 42 are not coupled to the gates of transistors 50 and 52. Accordingly, claim 8 is not anticipated by Lee.

Claims 9-10 depend on claim 8, and thus, are allowable for the same reasons that claim 8 is allowable. In addition, claim 9 recites that the compensation circuit includes a fourth transistor connected between a second mirror leg of a first current mirror and the control terminals of the first, second, and third transistors. An example of such a fourth transistor is the transistor Qc of Figure 5. Lee does not disclose such a fourth transistor. Instead, the transistors 40 and 42 are connected to the emitters, rather than the bases, of the transistors 50, 52. Accordingly, claims 9-10 are further distinguished from Lee.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Krishnamoorthy Ravishanker

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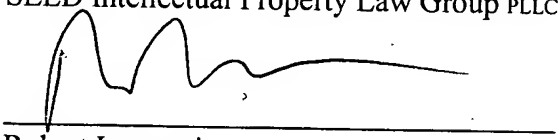

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